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10EC077

M.Tech. Degree Examination, December 2011
Synthesis and Optimization of Digital Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Draw the Y chart for different level of abstraction and synthesis. Explain different levels briefly. (10 Marks)

b. Implement 2 = a·b·c·d using two input AND or three input AND gates. Assume gate area and delays are proportional to the number of inputs. Draw the circuit and design space graph for 4 types of implementation. (06 Marks)

c. What are the various tasks performed in physical design? Explain briefly. (04 Marks)

2 a. Define the following with respect to concept of graph theory and write an example for each.
i) Directed graph ii) Hyper graph. (04 Marks)

b. What is meant by stability number and chromic number of a graph? Show that the graph shown in fig.Q2(b) is a perfect graph. (06 Marks)

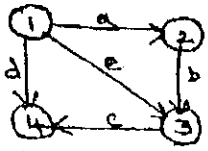

Fig.Q2(b)

c. Write Pseudo code for greedy scheduling algorithm and explain with an example. (10 Marks)

3 a. Write BDD for f = (a + b)c and obtain ROBDD for the same. (06 Marks)

b. Write silage code for recursive filter. (06 Marks)

c. Write data flow graph and sequencing graph for the model shown :

$a_1 = (3 * x + 4 * y) * (8 * z)$;

$b_1 = (8 * y) + 3$;

$c_1 = b1 \geq c$; $d_1 = 2 * x - 8$. (08 Marks)

4 a. Find minimum cover for the following function using exact logic minimization algorithm.
$f = \sum m_0, m_2, m_4, m_6, m_8, m_{10}, m_5, m_7, m_9, m_{11}, m_{13}$. (08 Marks)

b. Determine F^{ON}, F^{DC} and F^{OFF} set in positional cube notation for the function $f = a'b'c' + ab'c' + a'bc' + a'b'c$ with abc' as 0 don't care condition. Fund minimum cover using expand and reduce operator. (12 Marks)

5 a. Write Pseudo code for ASAP and ALAP used for scheduling. (10 Marks)

b. Obtain scheduled graph for the following model using list scheduling algorithm. Assume there are 3 multipliers and 1 ALU and unit execution delay.
a1 = x + dx ; a2 = u – (3 * x * u * dx) – (3 * y * dx) ;
a3 = y + u*dx a4 = a1 < b. (10 Marks)

6 a. A logic network has 5 primary inputs (a, b, c, d, e) and 4 primary outputs (w, x, y, z). The logic network is defined by
$p = ce + de$; $q = a + b$; $r = p + a'$; $s = r + b'$;
$t = ac + ad + bc + bd + e$; $u = q'c + qc' + qc$;
$w = v$; $x = s$; $y = t$; $z = u$; Obtain logic transformation elimination, decomposition and extraction. **(12 Marks)**

b. Compute Kernels and Co–Kernels based on matrix representation for $f = ace + bce + de + g$. **(08 Marks)**

7 a. For the state diagram, shown in fig.Q7(a), find minimum state diagram. **(10 Marks)**

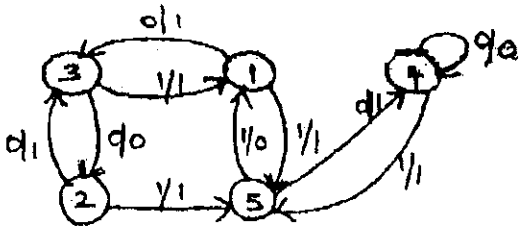

Fig.Q7(a)

b. Explain anyone ATPG method with neat diagram. **(10 Marks)**

8 Write short notes on :
a. Dijkstra algorithm.
b. ILP model for scheduling.
c. Tree based matching.
d. Rule based library binding. **(20 Marks)**

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